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Docket No.: 50253-118(P2287) **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :
AMIT GUPTA, et al. :
Serial No.: 08/868,972 : Group Art Unit: 2731
Filed: June 4, 1997 : Examiner: Brenda Pham
:

RECEIVED DEC - 1 1999 TECH CENTER 2700

For: TECHNIQUES FOR IMPROVING VIRTUAL CHANNEL MANAGEMENT AND MAINTENANCE IN A NETWORK ENVIRONMENT

THE COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Request for Reconsideration in the above identified application.

☒ No additional fee is required.

☐ Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified statement previously submitted.

☐ A verified statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.

☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	30	30	0	$18.00 =	$0.00
Independent Claims	10	10	0	$78.00 =	$0.00
		Multiple claims newly presented			$0.00
		Fee for extension of time			$0.00
					$0.00
				Total of Above Calculations	$0.00

☐ Please charge my Deposit Account No. 500417 in the amount of $0.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,
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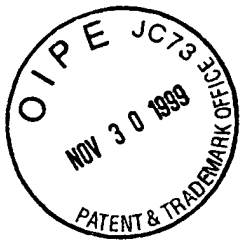

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For: TECHNIQUES FOR IMPROVING VIRTUAL CHANNEL MANAGEMENT AND MAINTENANCE IN A NETWORK ENVIRONMENT

REQUEST FOR RECONSIDERATION

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

This is in response to the Examiner's non-final Office Action of August 31, 1999. Claims 1-30 remain in the application. Claims 1-30 stand rejected. The independent claims are 1, 10-11, 17-18, 21 and 23-26.

Applicant respectfully requests reconsideration of the Examiner's rejections.

Rejections under 35 U.S.C. §112

The Examiner rejected claim 4 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. The Office Action states that the terminology "on less than all of the virtual circuits" is undeterminable (current Office Action, page 2).

The "less than all of the virtual circuits" terminology is explained in the specification. "In the prior art, there is sometimes a need to send keep alive packets or

refresh packets periodically over each virtual circuit to avoid a connection timing out and being broken down. With a virtual circuit bunch, one only needs to send one keep alive packet or refresh packet per virtual circuit bunch and not one for each circuit." (Specification, page 30, lines 18-24.) If only four virtual circuits in a virtual circuit bunch go to destination A, for example, then a refresh packet only needs to be sent on one of the virtual circuits. One is less than four.

Applicants respectfully submit this terminology is clear to one of ordinary skill in the art. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw the rejections of claim 4.

The current Office Action rejects claim 5 "due to depending on 35 U.S.C. 112 rejected claim" (current Office Action, page 13) then states "as set forth in claim 1." Applicants take this to mean "as stated in claim 4" which is the only claim rejected under 35 U.S.C. 112.

Applicants respectfully submit that because claim 5 depends on claim 4, claim 5 is allowable for the reasons given above for claim 4.

Rejections under 35 U.S.C. §103

The current Office Action rejects claims 1, 2, 6, 8 and 18-19 under 35 U.S.C. §103(a) as being anticipated by Dieudonne et al., U.S. Patent 5,793,766 (Dieudonne) in view of Nishihara et al., U.S. Patent 5,469,543 (Nishihara).

Applicants invention is directed to establishing and using together a set of pre-established virtual circuits of a network, such as an asynchronous transfer mode (ATM) network. "[A] group of virtual circuits [is] prestablished in a virtual circuit bunch" (VCB) (specification, page 23, lines 19-20). "Virtual Circuit Bunches [are] utilized to set-up and

manage together groups of virtual circuits in a flexible way which results in increased performance as well as overcoming the problems of the prior art." (Specification, page 4, lines 5-8.) As described in the specification "a hierarchy of aliases . . . [is] utilized to conveniently refer to portions of . . . a virtual circuit bunch," (specification, page 23, lines 17-20).

Advantages accrue to Applicant's invention from these features. For example, the "virtual path . . . defined in the ATM standard . . . 'contains' 2^{16} (65,536) virtual circuits . . . [and] requires significant additions to the ATM switch hardware" (specification, page 2, lines 21-24). The virtual circuit bunch (VCB) "enables groups of virtual circuits to be established . . . without any changes to switch hardware" (specification, page 4, lines 10-13). As another example, less network traffic is required to set up, use and break down the virtual circuit bunch (VCB) according to the invention, than is required to set up, use and break down each virtual circuit separately according to the prior art.

Dieudonne is directed to multiplexing information from a plurality of sources into a stream of asynchronous transfer mode (ATM) cells using "the same logical channel." (Dieudonne, Abstract.) Applicants respectfully submit that the logical channel of Dieudonne is just the virtual circuit known in the prior art and described in Applicants' specification. This is not changed by having, in the cell header, a two part name for the logical circuit, the name including a "virtual circuit group identifier" and a "virtual circuit identifier." The virtual circuit group identifier appears to be just the virtual path identifier known in the prior art. Thus Dieudonne does not teach or suggest the virtual circuit bunch of Applicants' invention.

In addition, Dieudonne does not teach or suggest the controller configured according to Appellants' invention. Unlike Dieudonne, in the present invention the controller of each switch is configured to set up a group of virtual circuits as a virtual circuit bunch. Also, unlike Dieudonne, the virtual circuit bunch (VCB) information of Applicants' invention is stored in tables on the controller of a switch involved in the virtual circuit bunch (VCB) in Applicants' embodiments, yet the "control unit" of Dieudonne's FIG. 6 is featureless, indicating the conventional control unit which does not have tables recording the virtual circuit bunch (VCB)s. The Examiner admits that Dieudonne "fails to explicitly teach the controller . . . configured to set up a group of virtual circuits to respective destinations as a virtual circuit bunch" (current Office Action, page 3).

The Office Action cites Nishihara for teaching "the above limitation" (current Office Action, page 3). Applicants respectfully submit that this is factually incorrect.

Nishihara teaches policing circuits in an ATM network to count the number of cells traversing on a given virtual path in order to enforce traffic constraints. Thus if a virtual path attempts to carry too many packets (cells) in an interval of time, the policing circuit will cut packets that exceed the allotted number, until the next time period begins. There is nothing to suggest that Nishihara is using anything but the prior art virtual path identifier in each cell to associate traffic with a virtual path. Nishihara does not address setting up or breaking down virtual circuits or virtual paths and does not teach or suggest virtual circuit bunches.

Specifically, Nishihara teaches "a VPI (virtual path identifier) detector 101 for detecting and extracting a VPI from the received cell. The extracted VPI is applied to . . .

a VPI-to-SC (service class) translation table 103. . . . A cell counter . . . updates the count value by incrementing the count in response . . ." (Nishihara, column 2, lines 40-49). "[The] translation table 103 produces a service-class identifier . . . and applies it to . . . a SC-to-threshold table 105 . . . [which] converts . . . into a corresponding upper limit value, or . . . 'contract value'," (Nishihara, column 2, line 53, to column 3, line 5). Then if "the count value would exceed the threshold value . . . processor 110 discards the cell" (Nishihara, column 3, lines 13-15).

Thus, Nishihara does not even address setting up or breaking down virtual circuits or virtual paths, and certainly does not teach virtual circuit bunches or a controller configured to set up a group of virtual circuits to respective destinations as a virtual circuit bunch.

Independent apparatus claim 1 recites "a virtual circuit bunch" and " a controller configured to set up at least one group of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by Dieudonne or Nishihara for the reasons given above. Therefore a rejection of claim 1 under 35 U.S.C. §103 is improper. Claims 2-9 depend, directly or indirectly, on claim 1, and are allowable for at least the same reason. The Examiner is requested to reconsider the rejections of claims 1, 2, 6 and 8.

Independent method claim 18 recites "a virtual circuit bunch" which is not taught or suggested by Dieudonne or Nishihara for the reasons given above. Therefore a rejection of claim 18 under 35 U.S.C. §103 is improper. Claim 19 depends on claim 18, and is allowable for at least the same reason. The Examiner is requested to reconsider the rejections of claims 18-19.

The current Office Action rejects claim 25 for the same reasons as set forth in claim 6, and rejects claim 29 for the same reason as set forth for claim 25 (current Office Action, page 13).

Independent claim 25 recites "a virtual circuit bunch" which is not taught or suggested by Dieudonne or Nishihara for the reasons given above. Therefore a rejection of claim 25 under 35 U.S.C. §103 is improper. Claim 29 depends on claim 25, and is allowable for at least the same reason. The Examiner is requested to reconsider the rejections of claims 25 and 29.

The current Office Action rejects claims 3 and 20 under 35 U.S.C. §103(a) as being anticipated by Dieudonne in view of Nishihara, and further in view of Hiller et al., U.S. Patent 5,345,445 (Hiller).

Hiller is directed to allocating data from several telecommunication calls into each cell transmitted over a virtual circuit. Hiller mentions "permanent virtual circuits (PVC)," and "a plurality of . . . PVCs is provisioned", and "only PVCs which have been activated can carry the signals for telecommunications calls" (Hiller, column 2, lines 18-28). However, this does not constitute the virtual circuit bunch (VCB) of Applicants' invention because the network does not treat them as a group.

Hiller does not teach how the PVCs are first set up or eventually broken down, or which processors or switches maintain a list of PVCs and their activity. Hiller only states that the "ingress node signals the egress node . . . the identification of the PVC" (Hiller, column 4, lines 21-27). Thus there is no showing that the PVCs of Hiller are not merely the virtual circuits and virtual circuit paths of the prior art, requested the same way and

managed the same way by the network. Hiller does not show the PVCs are set up by a controller configured to set up a group of virtual circuits as a virtual circuit bunch.

Also, there is only one such group. For example, if all PVCs are full, none are added, and the "system busy" condition occurs (Hiller, column 10, lines 23-26, and Figure 15, item 1216). Because there is only one group, there is no need for names of the group. Thus there is no "hierarchy of aliases . . . utilized to conveniently refer to portions of . . . a virtual circuit bunch," (specification, page 23, lines 17-20).

Only the source terminal knows how many PVCs have been set up and whether they are all busy or not. Only the source terminal applies the methods of FIGs, 15 and 16 of Hiller, cited by the Examiner. The switches in the rest of the network are not shown to treat the PVCs as a group. Thus a virtual circuit bunch (VCB) as that term is used in applicants' specification is not taught or suggested by Hiller.

Claims 3 and 20 depend on claim 1 which recites "a virtual circuit bunch" and " a controller configured to set up at least one group of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by Dieudonne or Nishihara or Hiller for the reasons given above. Because the combination does not teach or suggest every limitation of Applicants' claim, a rejection of claim 1 would be improper. Since claims 3 and 20 depend on claim 1, the rejection is also improper with respect to claims 3 and 20. The Examiner is requested to reconsider the rejection of claims 3 and 20.

The current Office Action rejects claims 7 and 19 under 35 U.S.C. §103(a) as being anticipated by Dieudonne in view of Nishihara, and further in view of Subramanian et al., U.S. Patent 5,519,707 (Subramanian).

Subramanian is directed to setting up virtual paths between a central management supervisor 202 and each of a set of switches in a network. (Fig. 6). On such a logical star arrangement, virtual circuit identifiers can be named by service type 704 and port ID (Fig. 7B). Subramanian uses permanent virtual paths as known in the prior art, but requests those paths from the central management supervisor 202. Specifically, Submaranian teaches a first "virtual service path [is] established between the first switch and the supervisor. Likewise, a second . . . virtual service path [is] established between the second [switch] and the supervisor" (Subramanian, column 3, lines 47-52). No details on setting up the virtual paths are given, so no suggestion is made that these virtual paths differ from the known prior art paths. Submaranian then teaches that "channel numbers within each service path are preassigned by the supervisor" (Subramanian, column 3, lines 55-56). Thus virtual circuit are not set up by the switch controllers themselves in bunches, as in Applicant's invention, but instead are set up in conventional ways by the supervisor.

Thus Subramanian does not teach or suggest virtual circuit bunches or switches with controllers configured to set up at least one group of virtual circuits as a virtual circuit bunch. Subramanian does not cure the deficiencies in Dieudonne or Nishihara.

Claim 7 depends on claim 1 which recites "a virtual circuit bunch" and " a controller configured to set up at least one group of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by Dieudonne or Nishihara or Subramanian for the reasons given above. Because the combination does not teach or suggest every limitation of Applicants' claim, a rejection of claim 1 would be improper. Since claim 7 depends on claim 1, the rejection is also improper with respect to claim 7.

Claim 19 depends on claim 18 which recites "a virtual circuit bunch" which is not taught or suggested by Dieudonne or Nishihara or Subramanian for the reasons given above. Because the combination does not teach or suggest every limitation of Applicants' claim, a rejection of claim 18 would be improper. Since claim 19 depends on claim 18, the rejection is also improper with respect to claim 19.

The Examiner is requested to reconsider the rejection of claims 7 and 19.

The Examiner rejected claim 9 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Nishihara and further in view of Suzuki, U.S. Patent 4,884,263 (Suzuki).

Suzuki is directed to packet switching in which two or more logical channels are set up in response to a request for a connection. "In the event of an abnormal condition in the first logical channel the message packets are re-routed to the second logical channel." (Suzuki, Abstract.) Suzuki teaches that the multiple logical channels are set up "in response to each call-setup control packet" and "[a]t the end of a call, all the virtual circuits are released by a call-clearing control packet" (Suzuki, column 3, lines 24-32).

Applicants respectfully submit that Suzuki does not teach or suggest that the multiple logical channels be pre-established before an individual call or persist beyond the duration of an individual call, as with a virtual circuit bunch (VCB). In fact, Suzuki teaches the opposite, that the multiple logical channels should be released upon completion of the call. Therefore, Suzuki does not teach or suggest a virtual circuit bunch (VCB).

Claim 9 depends on claim 1 which recites "a virtual circuit bunch" which is not taught or suggested by either Dieudonne or Nishihara or Suzuki for the reasons given

above. Because the combination does not teach or suggest every limitation of Applicants' claim, a rejection of claim 1 would be improper. Since claim 9 depends on claim 1, the rejection is also improper with respect to claim 9. The Examiner is requested to reconsider the rejection of claim 9.

The Examiner rejected claims 10, 21 and 22 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian.

Claim 10 recites "a virtual circuit bunch" and " a switching node to establish a plurality of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by either Suzuki or Subramanian for the reasons given above. Because the combination does not teach or suggest every limitation of Applicants' claim, a rejection of claim 10 is improper.

Claim 21 recites "a virtual circuit bunch" and "controllers . . . configured to set up at least one group of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by either Suzuki or Subramanian for the reasons given above. Because the combination does not teach or suggest every limitation of Applicants' claim, a rejection of claim 21 is improper. Since claim 22 depends on claim 21, the rejection is also improper with respect to claim 22.

The Examiner is requested to reconsider the rejections of claims 10, 21 and 22.

The current Office Action rejects claim 23 for the same reasons as set forth in claim 21, and rejects claim 27 for the same reason as set forth for claim 23 (current Office Action, page 13).

Independent claim 23 recites "a virtual circuit bunch" which is not taught or suggested by either Suzuki or Subramanian for the reasons given above. Therefore a

rejection of claim 23 under 35 U.S.C. §103 is improper. Claim 27 depends on claim 23, and is allowable for at least the same reason. The Examiner is requested to reconsider the rejections of claims 23 and 27.

The Examiner rejected claims 11-13 and 16-17 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian and further in view of Hiller.

Claim 11 recites "a virtual circuit bunch" and "establish a plurality of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by either Suzuki or Subramanian or Hiller for the reasons given above. Because the combination does not teach or suggest every limitation of Applicants' claim, a rejection of claim 11 is improper. Since claims 12-13 and 16 depend on claim 11, the rejection is also improper with respect to claims 12-13 and 16.

Claim 17 recites "a virtual circuit bunch" which is not taught or suggested by either Suzuki or Subramanian or Hiller for the reasons given above. Because the combination does not teach or suggest every limitation of Applicants' claim, a rejection of claim 17 is improper.

The Examiner is requested to reconsider the rejections of claims 11-13 and 16-17.

The Examiner rejected claims 14-15, 24 and 26 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian and further in view of Hiller and furthermore in view of Fisk, U.S. Patent 5,274,643 (Fisk).

Fisk is directed to a network "topology design process" which accounts for multiple node routing in response to policies that "minimize bandwidth consumption." (Fisk, Abstract.) Virtual circuits are "grouped into virtual paths" in the design process and not during any actual routing. Virtual paths are known in the prior art but are

different than virtual circuit bunches for the reasons given above. For example, virtual paths are defined between two nodes and do not allow for more than one destination as does a virtual circuit bunch. Nothing in Fisk suggests use of virtual paths other than those known in the art. In addition, Fisk does not even address actual routing in a network, but only addresses simulations of prior art routing for network design purposes. Applicants respectfully submit that Fisk does not teach or suggest a virtual circuit bunch as that term is used in Applicants' specification.

Furthermore, the Examiner does not provide an adequate technical reason or motivation to combine these references. Fisk is directed to designing a network and Hiller to packing cells on the network with telephone data. The Hiller, Suzuki and Subramanian networks already exist. None require the design methods of Fisk. Fisk does not profess a need for knowing how telecommunications data are packed into ATM packets. Therefore the Examiner has failed to establish prima facie obviousness, and a rejection under 35 U.S.C. §103 is improper.

Claims 14 and 15 depend on claim 11 which recites "a virtual circuit bunch" and "establish a plurality of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by either Suzuki or Subramanian or Hiller or Fisk for the reasons given above. Because the combination is not proper, and , in any case, does not teach or suggest every limitation of Applicants' claim, a rejection of claim 11 is improper. Since claims 14-15 depend on claim 11, the rejection is also improper with respect to claims 14-15.

Claim 24 recites "a virtual circuit bunch" which is not taught or suggested by either Suzuki or Subramanian or Hiller or Fisk for the reasons given above. Because the

combination is not proper, and, in any case, does not teach or suggest every limitation of Applicants' claim, a rejection of claim 24 is improper.

Claim 26 recites "a virtual circuit bunch" which is not taught or suggested by either Suzuki or Subramanian or Hiller or Fisk for the reasons given above. Because the combination is not proper, and , in any case, does not teach or suggest every limitation of Applicants' claim, a rejection of claim 26 is improper.

The Examiner is requested to reconsider the rejections of claims 14-15, 24 and 26.

The current Office Action rejects claim 28 for the same reasons as set forth in claim 24, and rejects claim 30 for the same reason as set forth for claim 26 (current Office Action, page 13). Claim 28 depends on claim 24, and is allowable for at least the reasons claim 24 is allowable, given above. Claim 30 depends on claim 26, and is allowable for at least the reasons claim 26 is allowable, given above. The Examiner is requested to reconsider the rejections of claims 28 and 30.

The Examiner also rejected claim 24 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian and further in view of Fisk.

Claim 24 recites "a virtual circuit bunch" which is not taught or suggested by either Suzuki or Subramanian or Fisk for the reasons given above. Because the combination is not proper, and , in any case, does not teach or suggest every limitation of Applicants' claim, a rejection of claim 24 is improper.

The Examiner is requested to reconsider the rejection of claim 24.

The current Office Action rejects claim 28 for the same reasons as set forth in claim 24 (current Office Action, page 13). Claim 28 depends on claim 24, and is

allowable for at least the reasons claim 24 is allowable, given above. The Examiner is requested to reconsider the rejections of claim 28.

The Examiner also rejected claim 26 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian and further in view of Hiller.

Claim 26 recites "a virtual circuit bunch" which is not taught or suggested by either Suzuki or Subramanian or Hiller for the reasons given above. Because the combination is not proper, and , in any case, does not teach or suggest every limitation of Applicants' claim, a rejection of claim 26 is improper.

The Examiner is requested to reconsider the rejection of claim 26.

The current Office Action rejects claim 30 for the same reason as set forth for claim 26 (current Office Action, page 13). Claim 30 depends on claim 26, and is allowable for at least the reasons claim 26 is allowable, given above. The Examiner is requested to reconsider the rejections of claim 30.

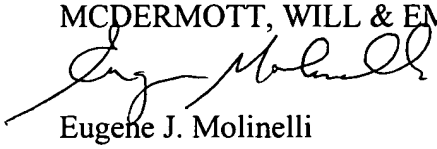
For the reasons given, Applicants believe that the application is in condition for allowance and the Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Should any additional issues remain that might be resolved by an interview or an Examiner's amendment, or if I can be of any assistance in any other way, please do not hesitate to contact me at (202) 756-8682.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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